



CV2AQ

Automotive Computer Vision SoC

Overview

Ambarella's AEC-Q100 qualified CV2AQ SoC combines image processing, 8MP30 video encoding, and CVflow® computer vision processing in a single, low-power design. The CV2AQ's CVflow engine's deep neural network (DNN) engine and a dedicated stereo vision accelerator enable efficient implementation of mono and stereo algorithms for the next generation of intelligent automotive cameras. Fabricated in advanced 10 nm process technology, it achieves an industry-leading combination of low-power and high-performance in both human vision and computer vision applications.

The CV2AQ's CVflow architecture provides computer vision processing at full 8MP resolution to enable image recognition over long distances and with high accuracy. It includes efficient 4K encoding in both AVC and HEVC video formats, delivering high-resolution video streaming with very low bit rates. The CV2AQ's next-generation image signal processor (ISP) provides outstanding imaging in low-light conditions while high dynamic range (HDR) processing extracts maximum image detail in high-contrast scenes, further enhancing the computer vision capabilities of the chip. It includes a suite of advanced security features to prevent hacking, including secure boot, TrustZone®, and key storage. A complete set of tools is provided to help customers easily port their own neural networks onto the CV2AQ SoC.



The CV2AQ chip targets automotive sensing camera designs

Key Features

Computer Vision Engine **CVflow**®

- Stereo processing to enable generic obstacle detection, terrain modeling, and more
- CNN- / DNN-based monocular processing to enable classification, tracking, and more
- Tools for high- and low-level algorithm development
- CNN toolkit for easy porting with Caffe, TensorFlow, and ONNX
- Open SDK

High-Efficiency Video Encoding

- H.265 and H.264 video compression
- Flexible multi-streaming capability
- 8MP30 video performance
- Multiple CBR and VBR bit rate control modes
- Smart H.264 and H.265 encoder algorithms

Ambarella Cutting Edge Imaging Pipeline

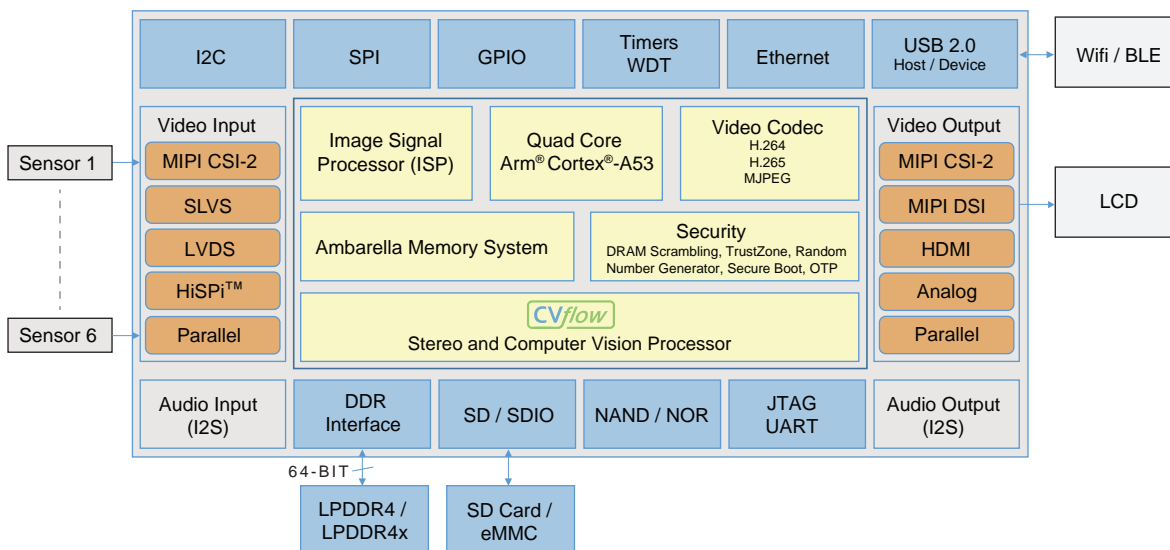
- Advanced imaging for low-light conditions
- LED flicker mitigation
- Wide dynamic range (WDR) and high dynamic range (HDR)
- Automotive multi-channel smart auto exposure and auto white balance

Target Applications

- Multi-channel drive recorder
- AVM / surround view with auto parking assist (APA)
- Single- / multi-channel eMirror
- ADAS
- Driver / cabin monitoring system (DMS / CMS)
- Short-range / long-range depth perception camera

Block Diagram

The diagram below illustrates a design based on the Ambarella CV2AQ device.



General Specifications

Processor Cores

- Quad-core Arm® Cortex®-A53 up to 756 MHz
- 32 KB / 32 KB I/D and 1 MB L2 Cache
- NEON™ SIMD and FPU acceleration
- OTP, secure boot, TrustZone®, IO virtualization
- AES / 3DES / SHA-1 / MD5 crypto acceleration

Video Input

- Hexa sensor input with independent ISP configuration
- Sub-LVDS / MIPI CSI-2 / SLVS / HiSPi™
- 16-bit parallel LVCMOS (BT.601 / 656)

Video Output

- 16-bit parallel LVCMOS (BT.601)
- HDMI® 2.0 including PHY with CEC support
- PAL / NTSC composite SD video
- MIPI DSI / CSI-2 and FPD (VESA / JEIDA)

CMOS Sensor Processing / Image Processing

- 8MP30 maximum input resolution
- Lens shading, fixed pattern noise correction
- Multi-exposure HDR (line-interleaved sensors)
- 3D motion-compensated temporal filtering (MCTF)
- RRGB / RCCB / RCCC / RGB-IR / monochrome sensor support
- Adjustable AE / AWB
- LED flicker compensation for LED sources
- Advanced dynamic range (WDR and HDR) engine
- Chromatic aberration correction
- 180° fisheye lens and geometric distortion correction
- OSD engine and overlays
- Gamma compensation and color enhancement
- Vignetting compensation
- 3-axis electronic image stabilization (EIS)
- Crop, mirror, flip, 90° / 270° rotation

Video Encoding

- H.265 MP L5.1, H.264 MP/HP L5.1, and MJPEG
- 8MP30 maximum encoding performance
- Up to 8 simultaneous stream encodes
- Flexible GOP configuration with I, P, and B frames
- Multiple CBR and VBR rate control modules

Computer Vision Processor

- **CVflow** processor with parallel architecture to boost performance of the low-level portion of perception algorithms
- Stereo matching
- Feature matching

Tools for Development

- CNN toolkit to ease the porting of CNN trained with Caffe, TensorFlow, or ONNX
- Compiler, debugger, and profiler for both Arm and Microcode development

Memory Interfaces

- LPDDR4x / LPDDR4 up to 1.4 GHz clock rate, 64-bit data bus, up to 4-Gbyte capacity
- Two SD controllers
- Boot from SPI / parallel SLC NAND with BCH / SPI NOR / USB / eMMC
- Single- / dual- / quad-SPI NOR and SPI NAND

Peripheral Interfaces

- One USB 2.0 port configurable as device / host w/PHY
- Audio interface including I²S
- Multiple SSI / SPI, IDC, and UART
- Multiple GPIO ports, PWM, Steppers, IR, ADC
- Watchdog timer, multiple general purpose timers, JTAG

Physical

- 10 nm low-power CMOS
- HS-BGA package (716 balls, 19x19 mm, 0.65 mm pitch)
- Operating temperature -40°C to +105°C
- Automotive qualified (AEC-Q100 Grade-2)

Computer Vision (CV) Applications

The CV2AQ vision processor enables different CV applications in different markets with its-state-of-the-art technology.

Perception Applications

- Driver and in-cabin monitoring system (DMS, CMS)
 - Driver drowsiness / distraction
 - Driver intent
 - Cabin monitoring
 - Driver authentication
 - Gesture control
- Object detection / classification (CNN-based)
 - Pedestrians, vehicles
 - Traffic signs, traffic lights
 - Headlight detection
- Free space detection
- Lane marking detection
- Parking lines detection

Enabled Computer Vision Applications

- Lane departure warning / lane keeping assistance
- Forward collision warning
- Auto emergency braking (AEB)
- Intelligent headlight control / high beam assist
- Speed assist functions
- Auto parking assist (APA)
- Blind spot detection

Stereo Computer Vision Functions

- Target tracking
- Generic obstacle detection
- Terrain modeling
- Curb and barrier detection

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